ACOUSTIC CHARGE TRANSPORT DIGITALLY PROGRAMMABLE TRANSVERSAL FILTER DEVELOPMENT

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ABSTRACT

A monolithic 128-tap digitally programmable analog transversal filter is described that uses an acoustic charge transport tapped delay line and integrated GaAs MESFET circuits for coefficient storage and tap weighting. The device has 5-bit tap weights, an input sampling rate of 360 MHz, and an output tap spacing corresponding to an output sampling rate of 180 MHz. The device is mounted on a ceramic thick film substrate along with RF input and output amplifiers and the entire assembly is housed in a 1.25 inch-square 44-pin kovar flatpack.

INTRODUCTION

Acoustic Charge Transport (ACT) technology has provided the basis for a new family of analog signal processors which include Programmable Transversal Filters (PTFs) [1]. Through monolithic integration of ACT delay lines with GaAs MESFET digital memory and programmable attenuators, these devices significantly extend the performance and improve the manufacturability of PTFs compared to those based on other signal delay technologies [2-8].

Recent development work on ACT PTF architectures has focused on chip size reduction to achieve better device yield and extension of function integration to reduce support circuit requirements thereby improving manufacturability of the complete hybrid assembly. At the same time, various performance parameters have been extended to address more stringent system requirements.

ACOUSTIC CHARGE TRANSPORT

ACT was first demonstrated by M. J. Hoskins and B. J. Hunsinger at the University of Illinois in 1982 [9]. Figure 1 is a cross-sectional view of a simplified ACT delay line and is used here to describe the basic ACT principle of operation.

A surface acoustic wave (SAW), generated by a high Q unidirectional transducer (UDT), propagates through a conductive region of a depleted n-doped GaAs epitaxial layer. This region is the acoustic charge transport channel. The traveling surface wave produces electric fields via the piezoelectric coupling of the GaAs crystal

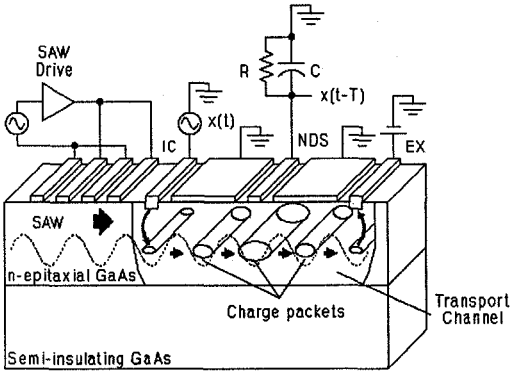

Figure 1. Simplified drawing of an ACT delay line.

which confine and transport charge injected into the depleted ACT channel at the input contact (IC) due to the input signal x(t). The charge propagates along with the traveling surface wave and electric fields past nondestructive sense (NDS) electrodes (only one shown here for simplicity) at the characteristic GaAs SAW velocity, 2864 m/s, to the charge extraction contact (EX). Each NDS tap then provides a delayed replica, x(t-T), of the input signal.

PTF FUNCTION

Figure 2 is a functional block diagram of a generic PTF which combines the basic transversal filter function (delay-multiply-accumulate) with adjustable tap weights and integral tap coefficient storage. This added capability allows PTFs to be constructed having many more taps than is practical using hybrid integration techniques. The filter function can be reprogrammed with new coefficients at any time during system operation. Such a filter can therefore perform many different jobs in the same system, including various adaptive operations, simply by altering the tap coefficients.

ACT PTF CHIP ARCHITECTURE

Figure 3 shows a simplified schematic of the ACT PTF chip architecture. The delay function is provided by an ACT delay line. The NDS electrodes in the ACT channel provide delayed signal replicas as inputs to programmable attenuators which perform the

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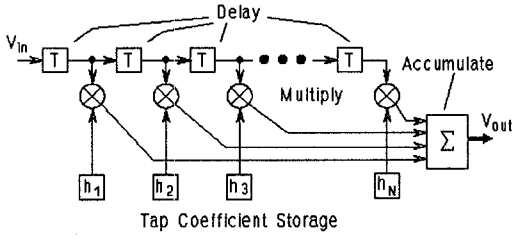

Figure 2. PTF functional block diagram.

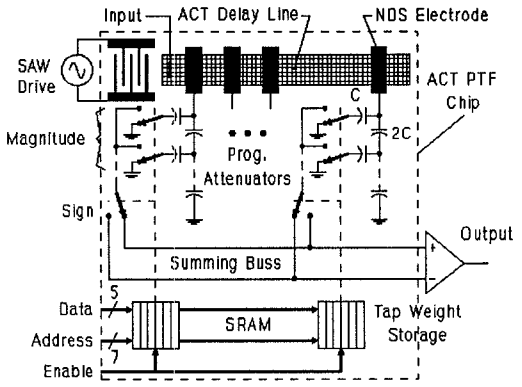

Figure 3. ACT PTF simplified schematic diagram.

multiplication operation. The summation function is provided by parallel connection of the outputs of all the programmable attenuators to a tap summing node. The tap coefficient storage is performed by GaAs static random access memory (SRAM).

The programmable attenuators are implemented by C-2C ladders as shown in Figure 4. These ladder networks act as multiplying digital-to-analog converters (MDACs) in that they effectively multiply the analog signal, shown entering the network on the left, by the digital word represented by DS and D3 through D0. The digital word is in signed-magnitude format where the DS bit represents the tap coefficient sign and D3 through D0 represents the tap coefficient magnitude. Each pair of GaAs RF transmission gates connected to the ladder branch output are driven by the Q and $\bar{Q}$ nodes of a single memory cell in the SRAM. This single-pole double-throw switch implementation allows the state of a magnitude memory cell to determine whether the signal current at a particular branch is sent to a summing node or to ground. The sign of the tap is determined by routing the signal current to either the noninverting or the inverting summing nodes by the DS memory cell and associated transmission gates. The digital word associated with each tap weights the tap signal current by any value between -1 and +1 in increments of 1/16.

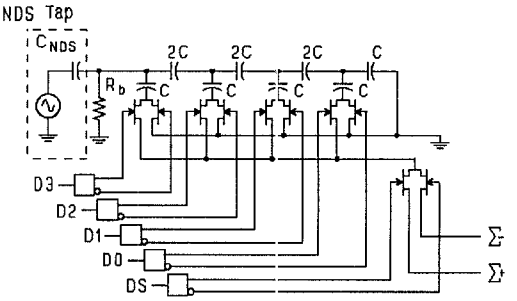

Figure 4. Schematic of the PTF tap weighting network.

The ACT PTF SRAM topology is shown in Figure 5. The only unique feature of this memory structure is that the state of each and every memory cell is constantly applied to the C-2C tap weighting networks. Data is written to a given memory location in a typical SRAM write operation, but because the stored data is always accessed by the ladder transmission gate connections, a specific read operation is unnecessary.

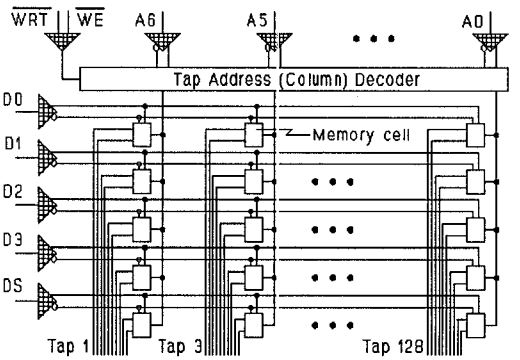

Figure 5. ACT PTF SRAM topology.

Figure 6 shows the ACT PTF chip layout. The 128 NDS taps are connected to their respective MDACs on alternating sides of the ACT channel. Since tap spacing is limited by the dimensions of the tap weighting circuits, this results in a smaller NDS tap spacing (5.6 nsec) which provides a larger operating bandwidth. The device SRAM is therefore split into two 5x64 arrays.

SUPPORT CIRCUITS AND HOUSING

The ACT PTF chip is mounted along with a silicon bipolar input amplifier, a GaAs differential output amplifier, a GaAs power FET, and 30 passive components on a 1 inch square alumina thick film

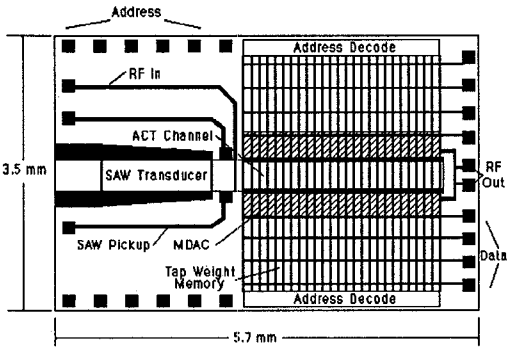

Figure 6. ACT PTF chip layout.

substrate, and housed in a 44-pin 1.25 inch by 1.25 inch by 0.125 inch kovar flatpack. The input amplifier is used simply to reduce module insertion loss while the differential output amplifier is needed to provide bipolar tap weights corresponding to the signed-magnitude coefficient format. The RF input and output signals are AC coupled and the various DC supply lines are RF bypassed. The GaAs power FET along with impedance matching circuit components make up a SAW delay line oscillator providing the energy to the SAW UDT . The thick film assembly and kovar flatpack is shown in Figure 7.

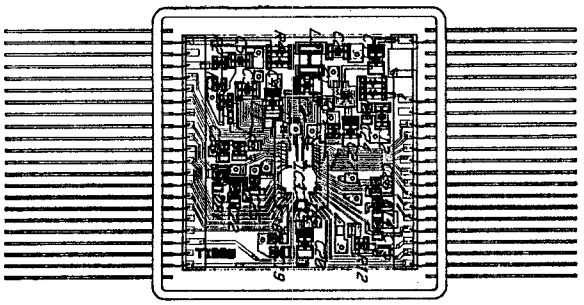

Figure 7. ACT PTF hybrid assembly.

ACT PTF PERFORMANCE

Two-tone dynamic range measurements show the ACT PTF module to possess greater than 45 dB spurious free dynamic range (SFDR) and 65 dB blocking dynamic range (BDR) when the device is programmed for the frequency and impulse responses shown in Figure 8. This response results from a full magnitude alternating sign pattern in the tap coefficients and provides the largest transfer function gain of any of the 32^{128} possible filter states. In this case the module insertion gain is roughly 10 dB. If a single tap coefficient is set to plus or minus one while all other tap coefficients are set to zero, the module insertion loss is roughly 15 dB. Figure 9 shows five superimposed time response plots for single taps programmed at various locations along the ACT channel.

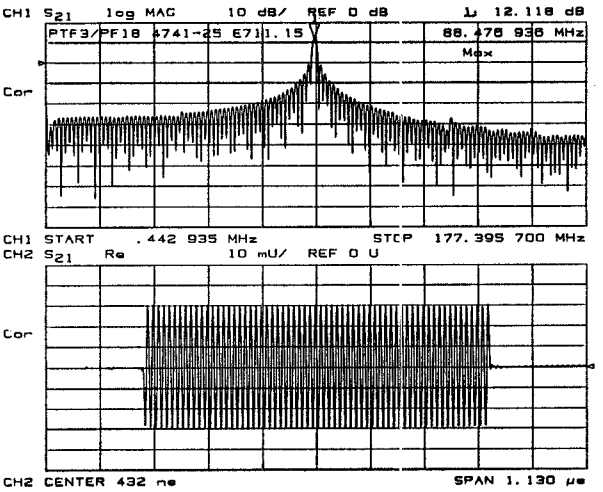

Figure 8. Alternating 1's pattern frequency and impulse response.

The data shown in Figure 10 contains both expected and measured frequency responses (S21 log magnitude) for a 128-tap 5-bit ACT PTF programmed to provide a hamming weighted 45 MHz passband response. The expected response was obtained by truncating the tap coefficients to 5 bits and performing a DFT on the rounded vector. Comparison of the two traces reveals that the device is providing 5 bits of overall accuracy which includes the accuracy of the individual MDACs and tap-to-tap uniformity.

Any tap weight coefficient can be reprogrammed in less than 1 µsec and the entire device can therefore be reprogrammed in less than 128 µsec. All digital inputs require 5 volt CMOS logic levels and all RF ports are matched to 50 ohms.

SUMMARY

We have demonstrated a programmable analog transversal filter based on ACT technology that extends prior PTF architectures to significantly wider

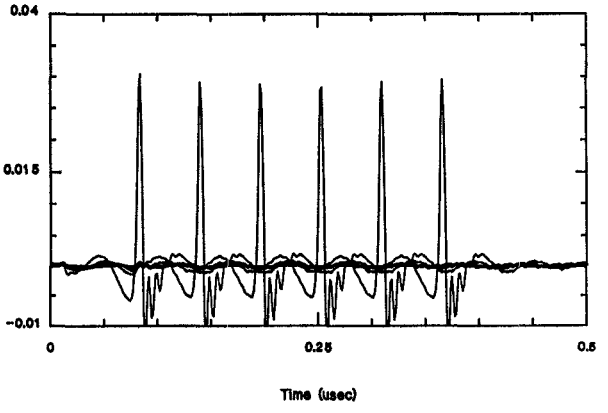

Figure 9. Single tap response.

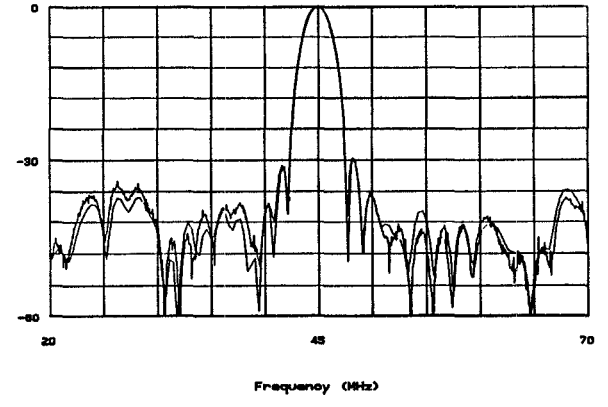

Figure 10. Expected and measured frequency response with 5-bit tap weight accuracy.

bandwidths. The device has 128 taps spaced by 5.6 nsec which can be independently set to weights extending from -1 to +1 in 5-bit increments. The tap spacing corresponds to an output sampling rate of approximately 180 MHz, which results in the effective execution of $2x10^{10}$ multiply and sum operations per second in an 0.16 cm^2 chip that dissipates less than 1.5 watts. The effective computation rate is limited in the present design by the spacing of the ACT delay line taps, which is dictated by the tap weight circuits.

Tap address and tap weight data are applied as parallel 7-bit and 5-bit words, respectively, and the data word is clocked into the address location by the application of an enable pulse. The tap weight circuits employ monolithic capacitors and GaAs MESFET analog switches to realize a multiplying D/A convertor based on a C-2C ladder configuration with a signed-magnitude tap weight word format. An overall ladder accuracy of 5 bits is achieved.

ACKNOWLEDGMENTS

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